X-BAND--GaAs FET YIG-TUNED OSCILLATOR

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Abstract

The results of an X-band GaAs FET YIG-tuned oscillator development are reported.

The best performance achieved was a minimum output power of 35 mW over the frequency range of 8.0 to 12.4 GHz with oscillations from 7.15 to 13.8 GHz.

Introduction

There have been many papers published concerning GaAs FET amplifiers, and a few papers reporting work on GaAs FET oscillators (references 1-6) in the microwave literature. Most of the oscillator work, however, has been concerned with narrow frequency band performance (references 1-5). This paper reports, for the first time, results of the development of full X-band (8.0 to 12.4 GHz) GaAs FET YIG-tuned fundamental oscillator. The approach used in this work was to utilize Avantek GaAs FET's with thin film MIC circuitry housed in a hermetically sealed magnetic structure. This oscillator is more efficient and has less input bias power consumption by an order of magnitude than equivalent Gunn diode-type X-band YTO's.

The advantages of this oscillator make it useful for sweeper, LO and EW applications, particularly where low power consumption is important. The unit also has sufficient output power to drive a single stage GaAs FET buffer amplifier to obtain output powers competitive with state-of-the-art X-band YTO's.

Technical Discussion

Device

The FET devices used in this work are made from liquid phase N-type GaAs epitaxial layer grown on semi-insulating GaAs substrates. The gate is a Cr-Pt Schottky Barrier with a gold overlay.

The mask geometry, as shown in Figure 1, was designed specifically for the common gate configuration used in this oscillator application. Typically, GaAs FET masks are designed with large source pads in order to obtain low common lead inductance, which is critical for common source amplifier applications. Our computer simulation studies and imperical observations have indicated that in order to achieve broader bandwidths and avoid unwanted resonant conditions, the source (as well as the drain and gate) pad should be as small as possible. The circuit layout chosen, as discussed later, dictated that the source and drain access should be on opposite sides of the FET chip. Figure 1, thus reflects these constraints as imposed on the FET geometry. The gate length is 1 μM and the total width is 500 μM. Typical S-parameters of the devices used in this work are shown in Figure 2. The measurements were made on unpackaged chips in the common source configuration (in order to be consistent with typical device measurement for comparison) using microstrip 50 Ω lines and microstrip to APC-7 adapters. The reference planes are at the device itself (plus bonding wires).

Circuit

The circuit design used in this work utilized unpackaged GaAs FET chips with an MIC thin film circuit. The circuit was then housed in a hermetically sealed (welded) magnetic structure. (See Figure 3) In order to operate up to 12.4 GHz and above, it was very important to reduce the stray circuit parasitics to a minimum. It is also important to provide a good heat sink for the FET in order to keep the device running as cool as possible, for maximum output power, and to maximize its reliability. In order to achieve this, the FET chip is mounted on a .010" thick BeO substrate, as shown in Figure 4. The basic configuration uses a short length of small wire connected from the gate bonding pad of the FET to ground serving as a feedback inductance, and a YIG-tuned tank circuit connected to the source pad. The output power is extracted from the drain, through a matching network. (See Figure 5 for schematic.) The FET chip is die attached with a gold-tin preform to a gold pad metallized on the BeO substrate. This pad is isolated from ground in order to reduce the total pad capacitance to ground of the source, drain, and gate bonding pads. The YIG loop is formed from a thin gold strap, attached to the source via a low capacitance gold pad on one end, and to a bypass capacitor on the other. The output circuit consists of a .010" thick sapphire substrate die attached to the BeO substrate. The output circuit contains the drain DC bias choke arrangement, the 50 Ω output line, and various output matching elements.

The conditions for oscillation for the GaAs FET in this configuration are analogous to that of the common base bipolar transistor case as discussed by Olliver (reference 7). The inductance in the gate lead causes the current to shift approximately 90°, thus producing a negative resistance at the source terminal. According to the Nyquist stability criteria, if the plot of the tank circuit impedance encircles clockwise the impedance looking into the source, the circuit is potentially unstable, and oscillations can occur. This is the case with this circuit, if the gate inductance is adjusted to place the negative resistance in the frequency range of interest. The YIG sphere used in this application was pure (undoped) YIG material with $4\pi M_s = 1780$.

Performance

The best results achieved with the oscillator described above is shown in Figure 6. As noted, the minimum power output was 35 mW over the 8.0 to 12.4 GHz region, with the unit oscillating from 7.15 to 13.8 GHz. It can be seen that the bandwidth is slightly less than an octave.

Larger bandwidths are achieved when the oscillator is tuned for lower frequency ranges (i.e., 6 to 13 GHz). The above results represents the best power achieved to date. However, the median minimum power obtained from other devices from this wafer and similar wafers is 10 to 15 mW

with similar bandwidths. The bias condition on this device was Vds = 6V, Ids = 50 mA.

The single side band FM noise measured on this oscillator was -63 dBc in a 1 KHz BW at 20 KHz from the carrier, measured at 10.5 GHz. The FM noise was measured by phase locking to a cavity stabilized low noise Gunn diode source and measured with a wave analyzer. This is approximately 15 to 20 dB higher noise than measured with Avantek bipolar transistor oscillators at this frequency, and about 5 to 10 dB more than a typical Gunn diode YTO. This GaAs FET oscillator noise performance is acceptable for many applications, such as high power sweepers, and EW applications Applications such as LO's for spectrum analyzers or synthesizers would require lower noise performance. It is felt that the noise performance of the GaAs FET's is dependent on the GaAs material. Optimization of material technology and oscillator circuits for low noise should improve the noise performance to approach the bipolar transistor results.

The second harmonic content was less than -24 dB below the carrier and the third harmonics were less than -30 dBc. The unit was exposed to heat sink temperature changes of 0°C to 65°C with a maximum measured frequency shift of 12 MHz and power variation of 1.5 dB. The GaAs FET oscillator is also capable of operating over more extreme temperature variations, such as those found in many military applications.

Conclusion

As a result of this work, it has been shown that GaAs FET's exhibit substantial output power in X-band. The DC to RF conversion efficiency is far superior to any full X-band oscillator available today. It is expected that the GaAs FET devices will steadily be improved, and consequently the outupt power and overall performance of the GaAs FET oscillator should increase significantly within the near future. It is also expected that GaAs FET oscillators will be operating over full Ku-band (12.4 to 18 GHz) with 10 mW or more output power within a short period of time.

References

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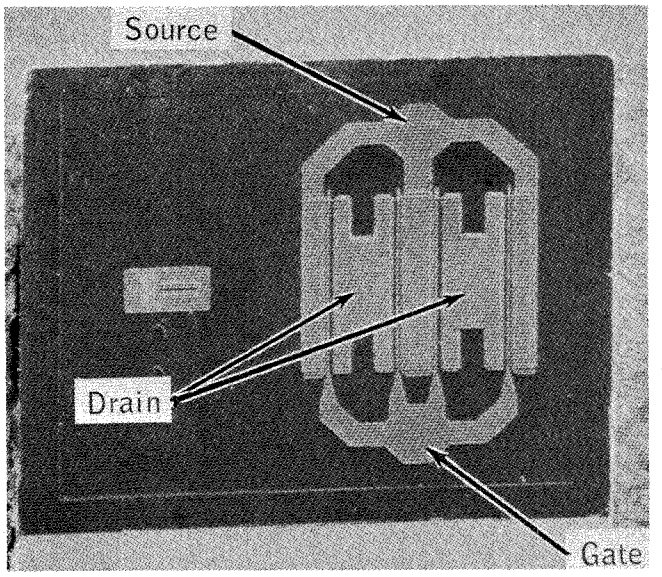

Figure 1

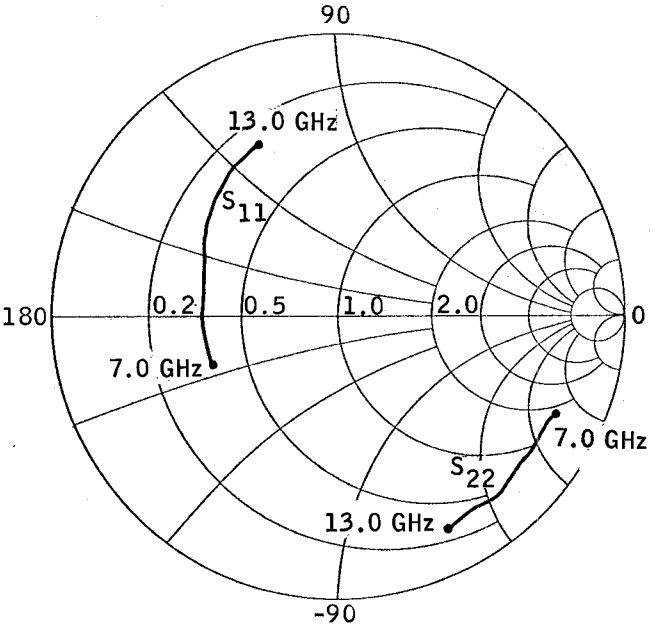

Figure 2

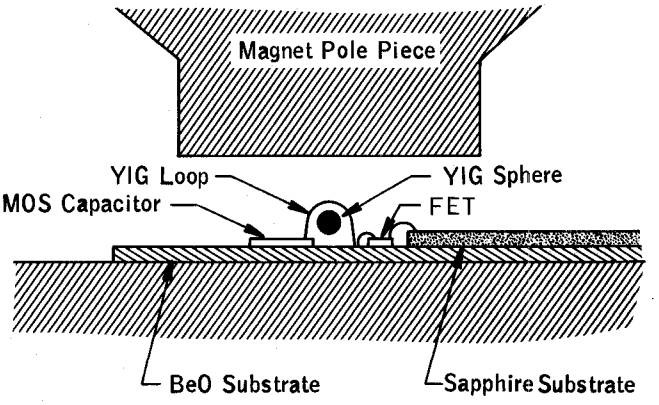

Figure 3 Oscillator Magnet Structure

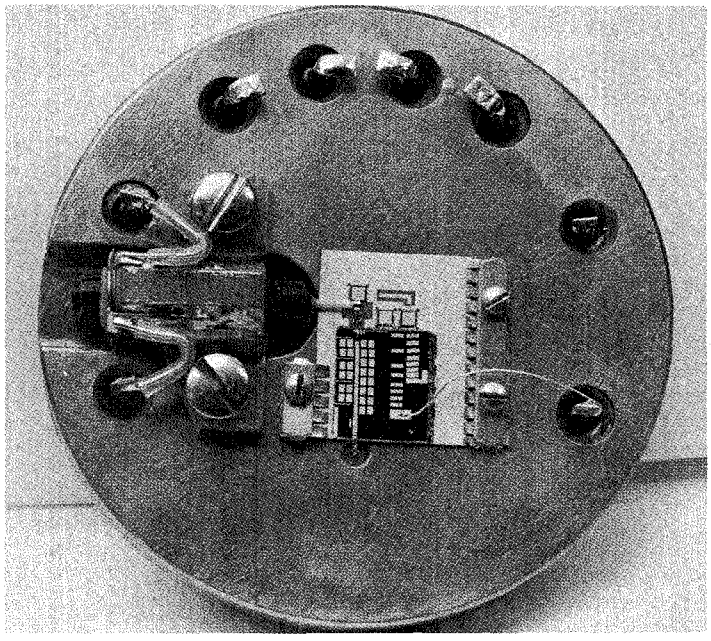

Figure 4

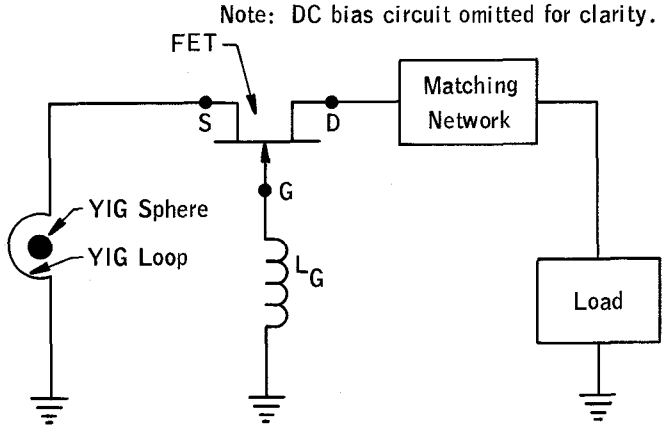

Figure 5 Oscillator Schematic

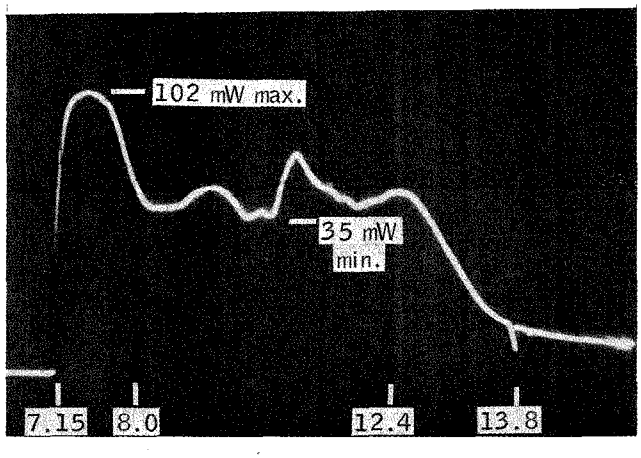

Figure 6